# STUDY OF SPACEBORNE MULTIPROCESSING FINAL REPORT - PHASE I

## Volume I
## Summary

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# FOREWORD

This final report describes the results of a study being conducted under National Aeronautics and Space Administration, Contract NAS 12-108, "Spaceborne Multi-Processor." The work is presented in two volumes, Volume I contains a summary of the study and Volume II a detailed technical discussion. The study is being performed by Data Systems Division of Autonetics, A Division of North American Aviation, Inc., Anaheim, California. The work is administered under the direction of the National Aeronautics and Space Administration, Electronics Research Center, Computer Research Laboratories, Cambridge, Massachusetts. Mr. F. Hills is the NASA project engineer.

The study began in March 1966. The contract participants included:

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# ABSTRACT

This final report presents a summary of the results of a research study of multiprocessing computer organizations and their application to future space missions. A manned Mars lander mission in the 1980 time period was investigated and computer requirements defined. Three multiprocessing computer organizations were developed: the multicompter, the modular multiprocessor, and the distributed processor. An evaluation of the three organizations resulted in the modular multiprocessor as the optimum candidate for the selected mission; this organization was then subject to a detailed design investigation.

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# I. SUMMARY OF THE STUDY

## 1.1 INTRODUCTION

The purpose of this study was to investigate multiprocessing computer organizations and their application to future space missions. A summary of the results of the study is given in this report; further information may be found in Volume II, the Technical Discussion Report.

## 1.2 REQUIREMENTS

Manned space missions in the 1980 time period were selected as the application area to be investigated. In order to establish a firm base for requirements, one mission in particular was selected for a detailed investigation, this was the manned Mars lander mission. This mission spans a broad spectrum of requirements (long duration, widely varying and diverse computational loads, high reliability demands, etc) so that using it as a base for requirements will result in applicability to many other missions in the same time period such as extended earth orbital space stations.

The manned Mars lander mission was subject to an extensive analysis to define the computational functions which then define the computer requirements. The mission profile covered a 420-day period and consists of three primary phases: Trans Mars, Mars Orbital, and Trans Earth. These three primary phases may be subdivided into twenty basic mission phases which begin with earth atmospheric ascent and culminate with earth re-entry; a listing of these twenty phases is given on the horizontal axis of Figures 1-1 and 1-2.

Computational functions may be broken down into four major types: (a) vehicle guidance and control, (b) telecommunications, (c) experiments data processing, and (d) system checkout. The mechanization of each of these four functions was investigated for each of the twenty mission phases. Based on these functions the computer requirements were defined for each phase. The computational storage and speed requirements as a function of mission phase are shown in Figures 1-1 and 1-2, respectively. It should be noted that the storage requirements are not shown as cummulative, i.e. these are the actual requirements for each phase only. If all the programs for the complete mission were stored in the computer at the onset of the mission the storage requirement would increase considerably; a non-cummulative storage requirement is achievable if a bulk storage device is available on board the vehicle. In addition, it should be pointed out that the requirements shown in the two figures do not include overhead functions such as executives, input/output, etc.; these functions result in approximately a 20-percent increase in the requirements.

There are two other requirements which were defined for the computer. The first is a reliability requirement; a probability of success of 0.997 and an availability of 0.997 are required. Secondly, a reconfiguration time of 5 seconds is required during critical computations. Reconfiguration is defined as having the computational function mechanized and being performed correctly in the computer system after some failure in the computer system. Critical computations are those that affect crew safety such as atmospheric entry guidance and control.

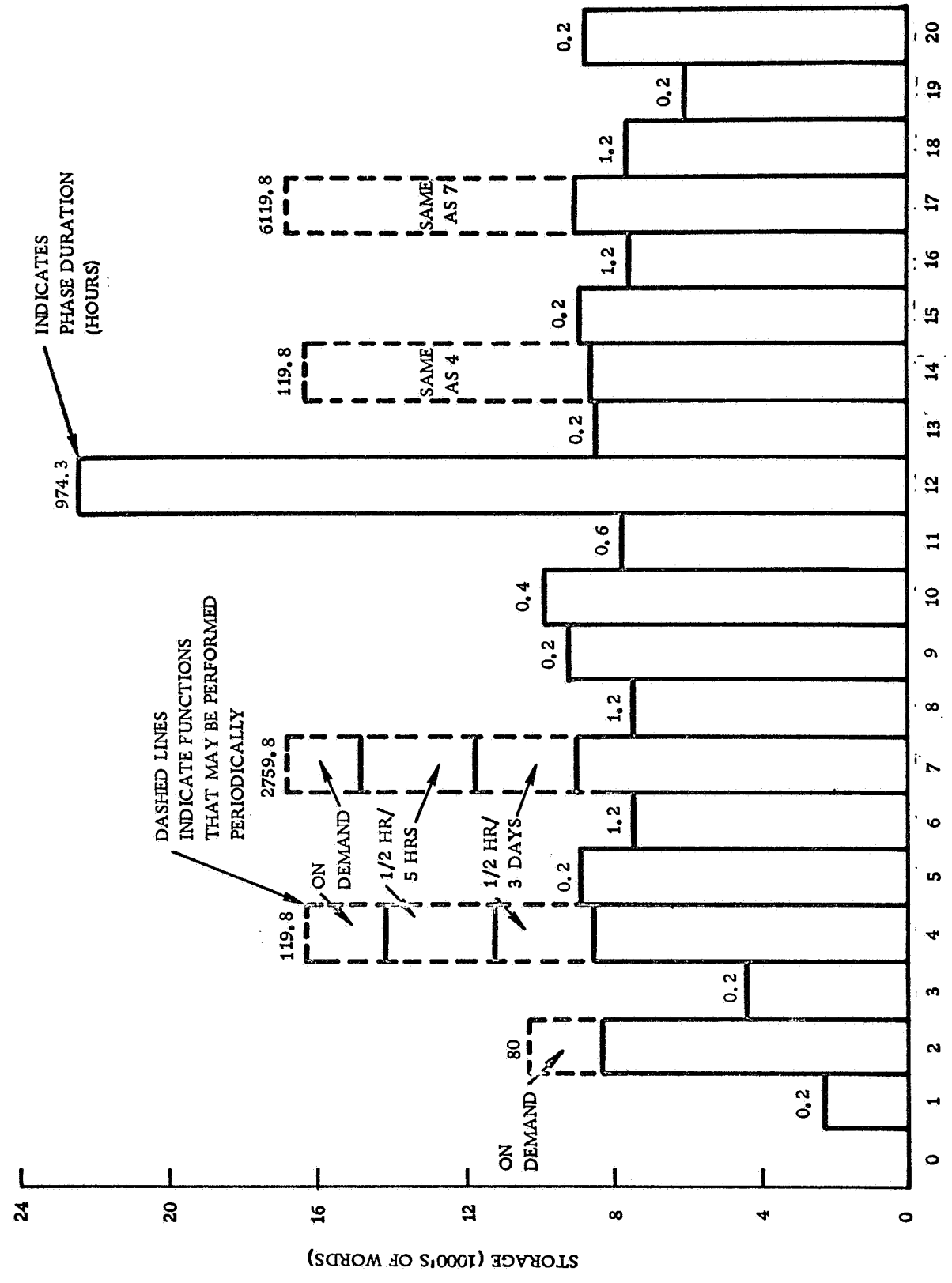


Figure 1-1. Mission Storage Requirements

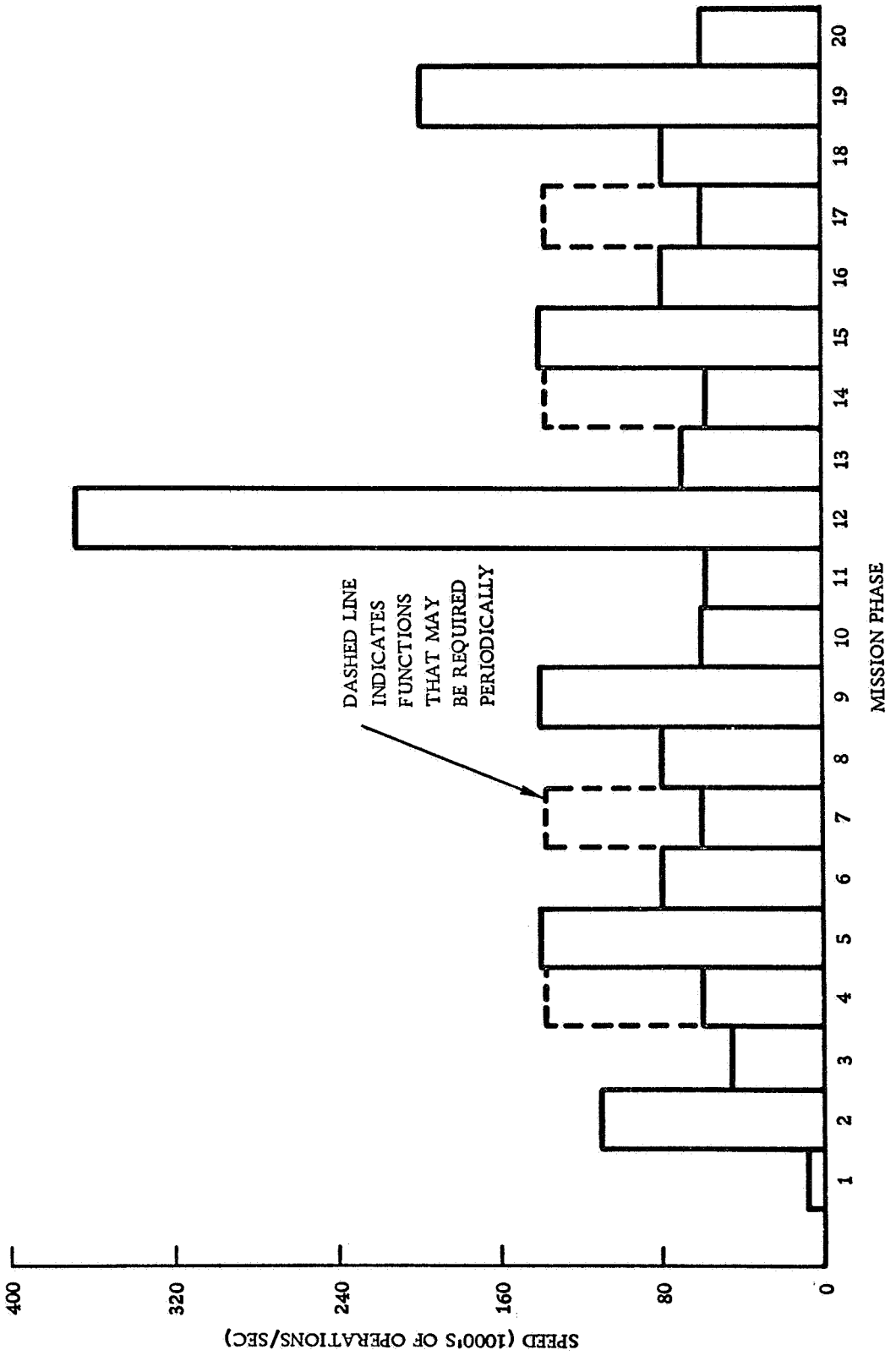


Figure 1-2. Mission Speed Requirements

## 1.3 TECHNOLOGY

In addition to defining the requirements, it was necessary to define the technology to be considered as state of the art for the time period of interest before proceeding with an investigation of multiprocessor organizations. For the time period of the missions considered, it is necessary to use technology that will be available to designers in the 1975 time period.

It is difficult to predict the most applicable technology at the end of the next 8 years under the dynamic conditions currently experienced in technology trends. The approach taken was to examine technology currently under development, use its functional characteristics for design, and extrapolate its physical characteristics to 1975.

The circuit technology selected for the time period of interest is MOS-SOS (Metal Oxide Semiconductor - Silicon on Sapphire). Densities for these circuits are expected to be 5,500 FET'S (Field Effect Transistors) per 150 mils square chip with operation at a five megahertz clock. It should be noted that these are considered to be quite conservative estimates and therefore, readily achievable as a proven technology by the required development time.

Two types of memory technology are considered for the time period of interest, a NDRO magnetic memory and a NDRO semiconductor (MOS-SOS) memory. The magnetic memory is expected to offer a lower development risk and the semiconductor memory a lower power dissipation with regards to relative advantages between the two appraches.

## 1.4 MULTIPROCESSOR CANDIDATES

Multiprocessing organizations are considered to offer considerable advantages in application to the requirements of future manned space missions. These organizations can result in: (a) efficiently meeting the widely varying computational loads of different phases of a mission, (b) efficiently mechanizing the diverse requirements of various subsystems of a mission such as a command module and a lander module, (c) an overall net reduction in power due to the ability to turn modules on and off, (d) an increase in reliability, given that failure rates of dormant equipment are lower than operating equipment, and (e) enhancement of probability of mission success and availability with the potential of graceful degradation of the computation system due to reconfiguration around failures at a low module level.

Using the requirements and technology as a base, three organizational approaches to multiprocessing were investigated. These were: (a) multicomputer, (b) modular multiprocessor, and (c) the distributed processor.

Prior to a preliminary design of each of these candidates, an evaluation of computer features in general was conducted. An 18-bit instruction word was selected. This instruction word provides the features desired and is a convenient data size (single precision on most computations and double precision on some guidance and control functions). Double indexing/banking is provided with nine full length index/bank registers, these registers may be used to index/bank with one of two specific registers taken with one or none of seven other registers. Two accumulators are used, this provides considerable efficiency in handling certain programs. Indirect addressing is provided as a separate bit in the instruction word. It is possible to implement multi-level indirect

addressing with the indirect word format selected. It should be mentioned that the above features are only really applicable to the first two candidates, the multicomputer and the modular multiprocessor. The distributed processor is a rather unique organization and time did not permit an investigation of such features for this organization.

### 1.4.1 Multicomputer

The multicomputer organization consists of two independent computers each with a 250,000 operation per second processor, a 24,000-18 bit word memory (capable of being turned on/off in 12,000 word modules), and a program controlled input/output section. The individual computers perform self-checks and are interconnected so that critical system outputs can be automatically switched from a failed computer to a correctly operating computer through an output switch. The computers are turned on and off to meet the particular requirements of each mission phase, in addition, some of the 12,000 word memory sections are turned on and off as the requirements vary.

### 1.4.2 Modular Multiprocessor

A block diagram of the modular multiprocessor organization is shown in Figure 1-3. It consists of two 250,000 operations per second processors, three 12 12,000-18 bit word memories, and two input/output modules with full intercommunication between the memories and processors and between the memories and input/output modules. It should be noted that Figure 1-3 shows the ability to expand to four memories, three processors, and three input/output modules as indicated by the modules in dotted lines. This prevents the failure of one processor-memory system from annihilating information in memories or in disturbing the operation of the remainder of the computer system. As in the multicomputer organization the modules are turned on and off to meet the requirements of the various phases; the difference here is that the modules are now at a lower level, thereby offering a closer match to varying requirements.

### 1.4.3 Distributed Processor

A block diagram of the distributed processor organization is shown in Figure 1-4. This type of multiprocessor contains a decentralization of the logic elements on an array basis. The organization was designed to take advantage of applied and natural parallelism in computational functions. It consists of a number of groups of cells all

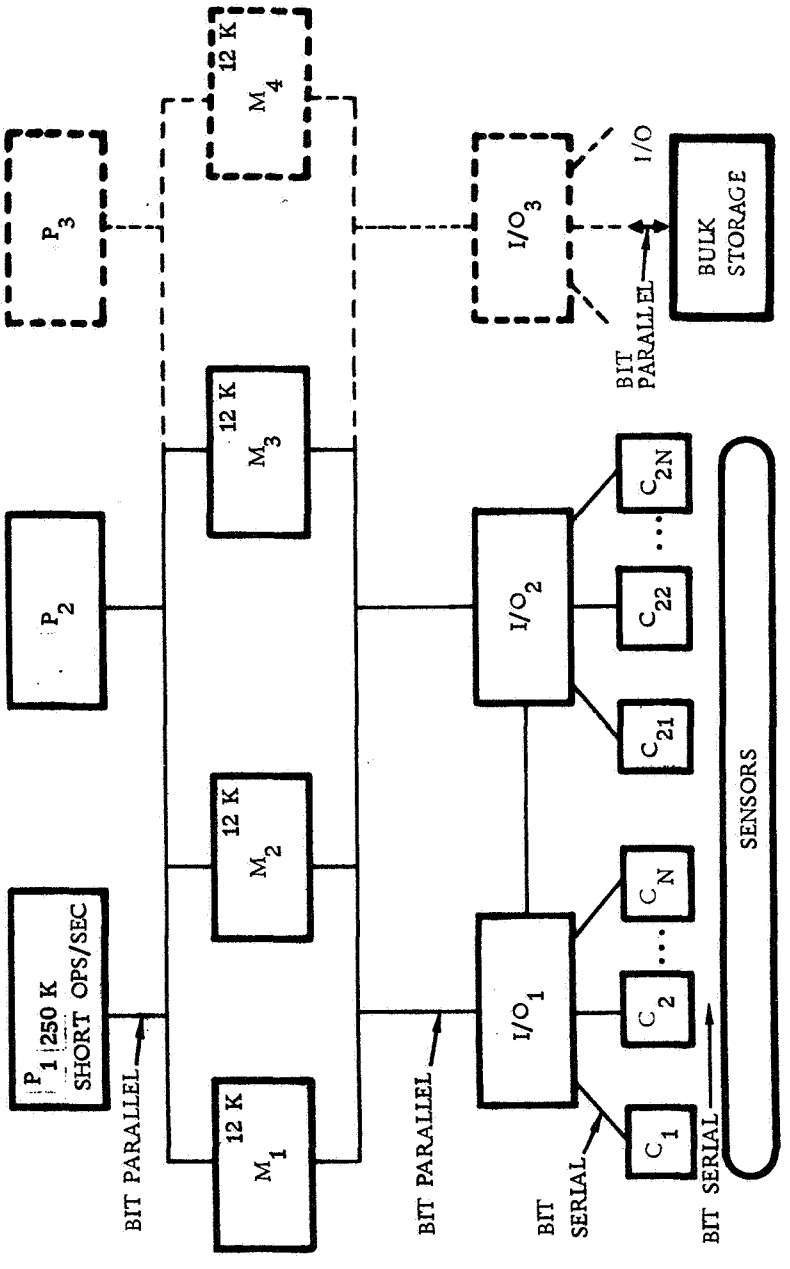


Figure 1-3. Modular Multiprocessor

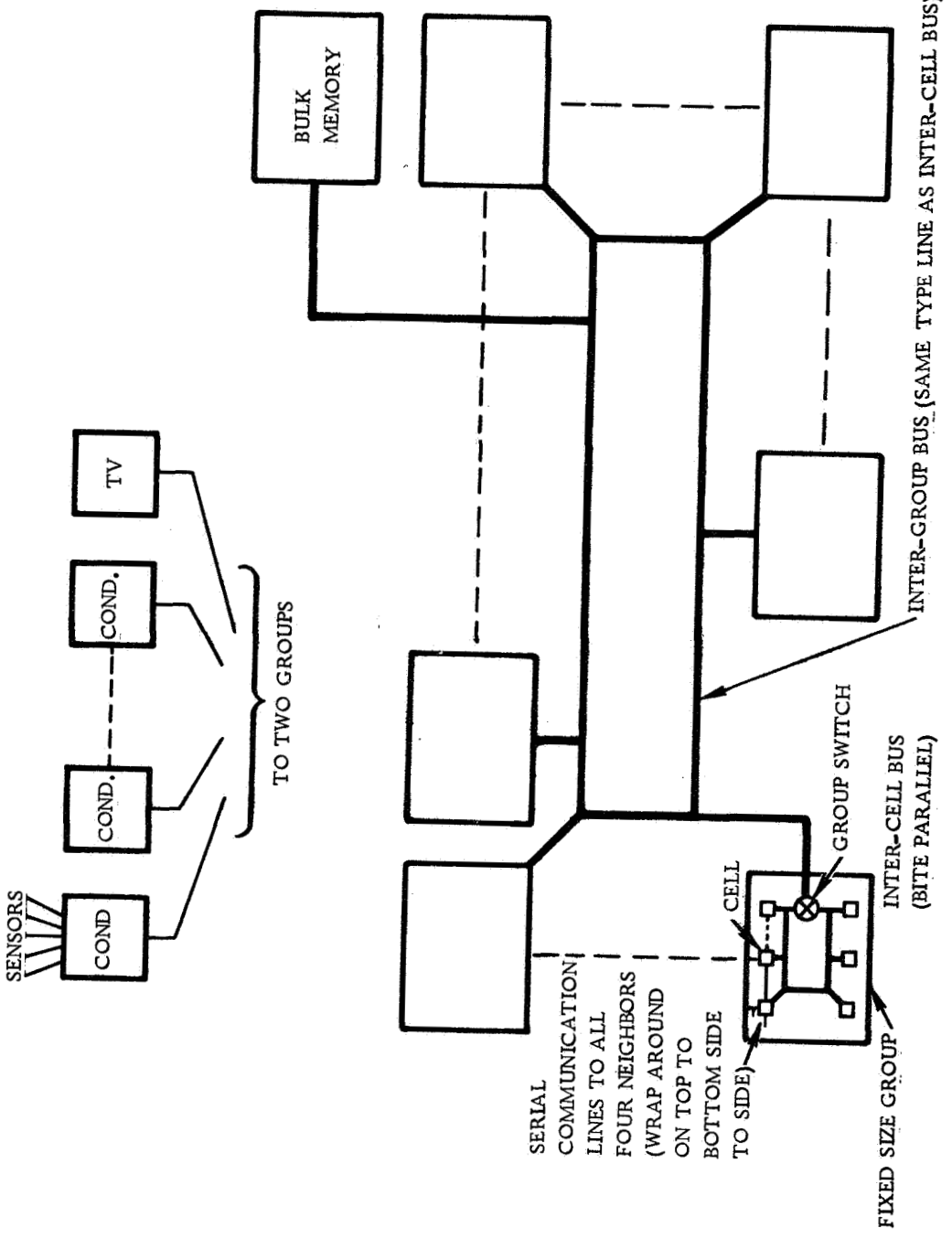


Figure 1-4. Distributed Processor

parallelism in computational functions. It consists of a number of groups of cells all interconnected through an inter-group bus. Each cell in a group executes macro instructions from storage or from a controller cell within the group and can communicate to its neighboring cells. The cells are all identical and contain control, logic, and storage. These cells are organized into fixed size groups each of which can perform a computational task, one of these groups would normally be set aside to act as an overall executive. Due to the fine degree of modularity involved in this organization, it is possible to closely match the computer resources in use to the requirements. The maximum number of groups required for this mission is 25 and each group consists of 25 cells. This organization provides what may be considered as graceful degradation, for as cells begin to fail only a small portion of the computation resources are lost thereby resulting in only a small amount of computational functions that may have to be suspended. It should be mentioned that the three organizations discussed above span what may be considered organizations that may be implemented with today's technology to those possible a decade away (Distributed Processor).

## 1.5 SIMULATION AND EVALUATION

Using the results of the preliminary design of the three candidates, a simulation (reliability) and critical evaluation was performed. A Monte Carlo reliability analysis program was used to simulate the reliability performance of each of the candidates for the entire length of the mission. Analytical expressions were developed for the error in the probability of success($P_S$) obtained from the Monte Carlo program. The errors were found to be considerably lower than expected (e.g. error in $P_S = 0.0047$ for a $P_S$ of 0.95 with a 95 percent confidence level).

Figure 1-5 shows the probability of success curve for the modular multiprocessor. It can be seen that the requirements are met ($P_S = 0.997$) with 2 spare memory modules, 1 processor, and 1 input/output module. the ratio of relative failure rates between operating equipment and dormant equipment ($\lambda$on/$\lambda$off) is a very important parameter when considering probability of success. The effects of this ratio on the multicomputer candidate are shown in Figure 1-6. It can be seen that there are very significant gains on $P_S$ between the $\lambda$on/$\lambda$off ratios from 1 to 10.

In order to evaluate the candidate multiprocessing organizations, the computer system characteristics were weighted in terms of relative importance as follows: (a) Computer Probability of Mission Success - 100, (b) Power - 10, (c) Growth Potential - 4, (d) Development Risk - 1, (e) Weight -1, (f) Size - 1, (g) Cost - 1. From the results of the evaluation the modular multiprocessor was selected for further investigation.

## 1.6 MODULAR MULTIPROCESSOR DESIGN

The modular multiprocessor described above was subject to a detailed investigation in terms of module design, fault detection, and software design.

Each of the three modules, the processor, memory, and I/O was investigated further. With regards, the processor module, the real time clock, and interrupt system were functionally designed.

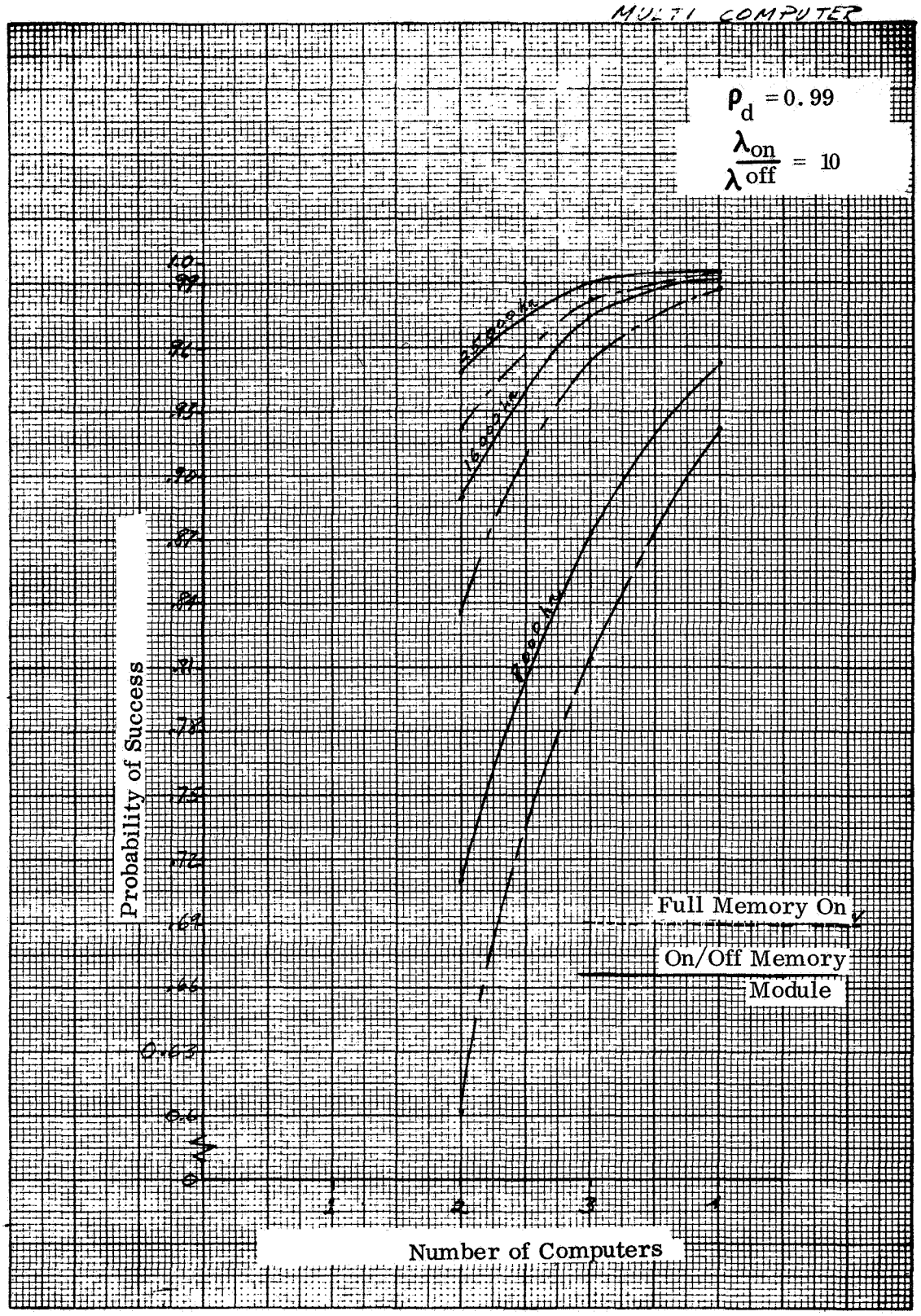


Figure 1-5. Modular Multiprocessor Probability of Success

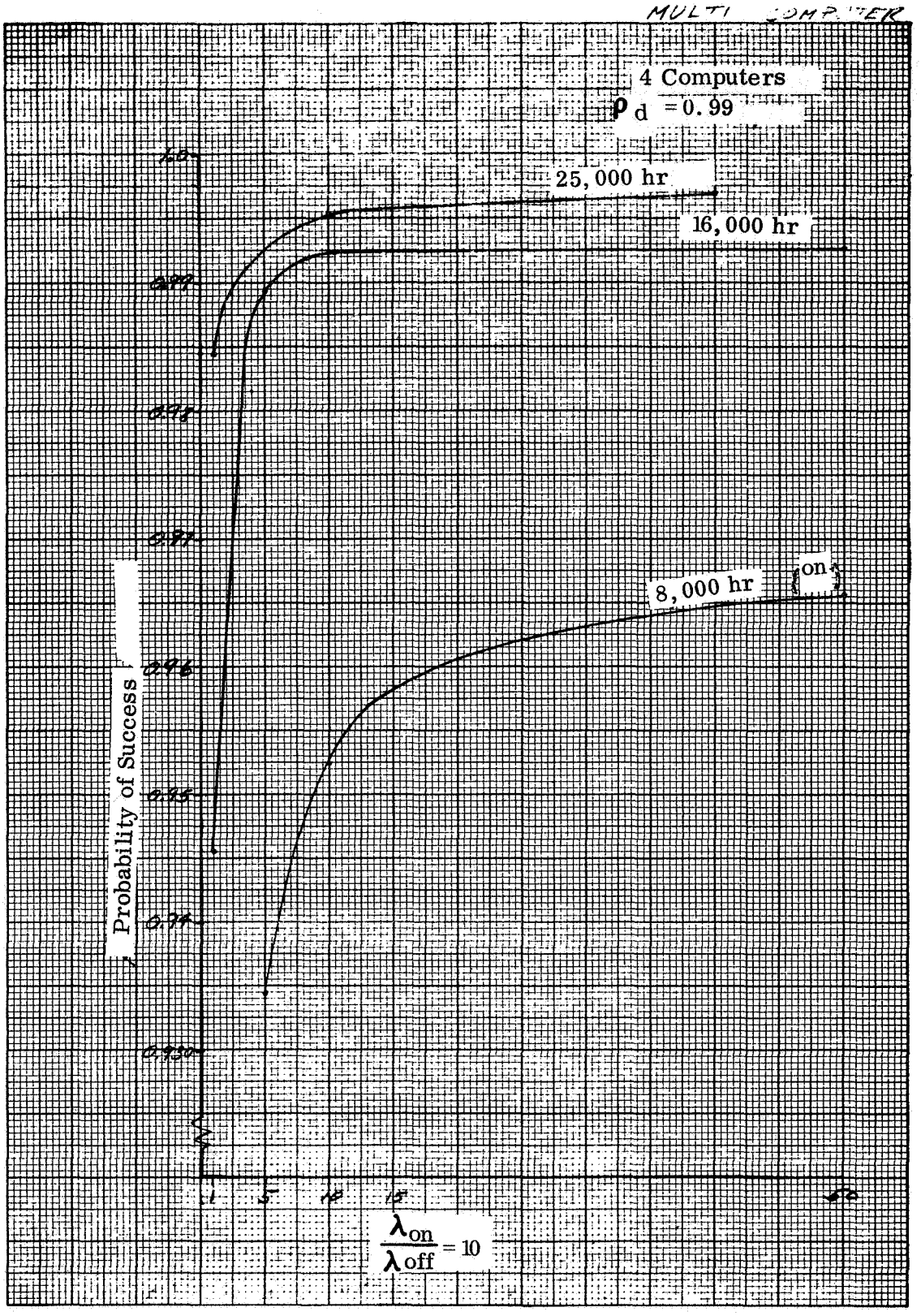


Figure 1-6. ON/OFF Failure Rate Effects on $P_s$

A complete instruction set was developed. The interface between the memory was designed and a detailed block diagram of the processor module was developed.

A detailed investigation of both the semiconductor (MOS-SOS) and Magnetic (NDRO multiword) memories was carried out. A detailed block diagram along with reliability and power estimates was derived. Similarly, a detailed diagram and functional description of the I/O module was developed. The next stage in the design of these modules would be detailed timing diagrams and development of logic equations.

Each of the modules was subject to an investigation of fault detection methods. Both software and hardware methods were considered. Further data is needed on intermittent type of failure modes in order to permit a tradeoff between the two methods of fault detection.

A software investigation of this organization was carried out and detailed executive flow charts were developed.